AMENDMENTS TO THE CLAIMS

Claim 1 (Previously Presented): A signal processing apparatus, comprising:

a channel pooling signal processor, including:

a reconfigurable multiprocessor having a plurality of computation units and an interconnect mechanism, each computation unit having a data sequencer for controlling program execution, a configurable logic unit, and a dedicated memory;

a test interface for testing the function of said plurality of computation units; and

a general purpose microprocessor for managing data flow into and out of said channel pooling signal processor;

wherein the interconnect mechanism connects said plurality of computation units, said test interface, and said general purpose microprocessor; and

a digital signal processor connected to said channel pooling signal processor;

wherein said channel pooling signal processor performs more computationally intensive signal processing operations and said digital signal processor performs less computationally intensive signal processing operations.

Claim 2 (Deleted)

Claim 3 (Original): The signal processing apparatus of Claim 1, further comprising:

a second channel pooling signal processor for processing multiple data streams of voice and data information.

Claim 4 (Original): The signal processing apparatus of Claim 1, wherein said plurality of computation units are heterogenous computation units.

Claim 5 (Original): The signal processing apparatus of Claim 1, wherein said plurality of computation units are homogeneous computation units.

Claim 6 (Previously Presented): A method for signal processing, comprising the steps of:

processing high complexity algorithms in a channel pooling signal processor, said channel pooling signal processor including:

a reconfigurable multiprocessor having a plurality of computation units and an interconnect mechanism, each computation unit having a data sequencer for controlling program execution, a configurable logic unit, and a dedicated memory;

a test interface for testing the function of said plurality of computation units; and

a general purpose microprocessor for managing data flow into and out of said channel pooling signal processor;

wherein the interconnect mechanism connects said plurality of computation units, said test interface, and said general purpose microprocessor; and

processing low complexity algorithms in a digital signal processor connected to said channel pooling signal processor.

Claim 7 (Original): The method of Claim 6, further comprising the steps of:

controlling program execution in a computation unit of said plurality of computation units;

configuring a configurable logic unit in said computation unit in accordance with a standard; and

storing program execution instructions in a dedicated memory in said computation unit.

Claim 8 (Original): The method of Claim 6, further comprising the steps of.

processing multiple data streams of voice and data information in a second channel pooling signal processor.

Claim 9 (Previously Presented): A base station transceiver comprising:

an antenna for receiving communication signals; and

a signal processing apparatus having:

a channel pooling signal processor, including:

a reconfigurable multiprocessor having a plurality of computation units and an interconnect mechanism, each computation unit having a data sequencer for controlling program execution, a configurable logic unit, and a dedicated memory;

a test interface for testing the function of said plurality of computation units; and

a general purpose microprocessor for managing data flow into and out of said channel pooling signal processor;

wherein the interconnect mechanism connects said plurality of computation units, said test interface, and said general purpose microprocessor; and

a digital signal processor connected to said channel pooling signal processor;

wherein said channel pooling signal processor performs more computationally intensive signal processing operations and said digital signal processor performs less computationally intensive signal processing operations.

Claim 10 (Previously Presented): A method for processing communication signals, comprising the steps of:

receiving communication signals;

processing high complexity algorithms on the received communications signals in a channel pooling signal processor, said channel pooling signal processor including:

a reconfigurable multiprocessor having a plurality of computation units and an interconnect mechanism, each computation unit having a data sequencer for controlling program execution, a configurable logic unit, and a dedicated memory;

a test interface for testing the function of said plurality of computation units; and

a general purpose microprocessor for managing data flow into and out of said channel pooling signal processor;

wherein the interconnect mechanism connects said plurality of computation units, said test interface, and said general purpose microprocessor; and

processing low complexity algorithms in a digital signal processor connected to said channel pooling signal processor.

Claim 11 (Previously Presented): The signal processing apparatus of Claim 1, wherein the computation units are flexibly configured and connected to perform any one of several different transceiver functions.

Claim 12 (Previously Presented): The signal processing apparatus of Claim 1, wherein the computation units are configured to perform one or more of downconversion, dechannelization, demodulation, decoding, equalization, despreading, encoding, modulation, spreading, and diversity processing.

Claim 13 (Previously Presented): The signal processing apparatus of Claim 1, wherein the computation units support time-division, code-division, and/or frequency division processing.

Claim 14 (Previously Presented): The method of Claim 6, wherein the computation units are flexibly configured and connected to perform any one of several different transceiver functions.

Claim 15 (Previously Presented): The method of Claim 6, wherein the computation units are configured to perform one or more of downconversion, dechannelization, demodulation, decoding, equalization, despreading, encoding, modulation, spreading, and diversity processing.

Claim 16 (Previously Presented): The method of Claim 6, wherein the computation units support time-division, code-division, and/or frequency division processing.

Claim 17 (Previously Presented): The base station transceiver of Claim 9, wherein the computation units are flexibly configured and connected to perform any one of several different transceiver functions.

Claim 18 (Previously Presented): The base station transceiver of Claim 9, wherein the computation units are configured to perform one or more of downconversion, dechannelization, demodulation, decoding, equalization, despreading, encoding, modulation, spreading, and diversity processing.

Claim 19 (Previously Presented): The base station transceiver of Claim 9, wherein the computation units support time-division, code-division, and/or frequency division processing.

Claim 20 (Previously Presented): The method of Claim 10, wherein the computation units are flexibly configured and connected to perform any one of several different functions of the base station transceiver.

Claim 21 (Previously Presented): The method of Claim 10, wherein the computation units are configured to perform one or more of downconversion, dechannelization, demodulation, decoding, equalization, despreading, encoding, modulation, spreading, and diversity processing.

Claim 22 (Previously Presented): The method of Claim 10, wherein the computation units support time-division, code-division, and/or frequency division processing.

Claim 23 (New): A signal processing apparatus, comprising:

a channel pooling signal processing means, including:

a reconfigurable multiprocessing means having a plurality of computing means and an interconnect means, each computing means unit having a data sequencing means for controlling program execution, a configurable logic means, and a dedicated memory;

a testing means for testing the function of said plurality of computing means; and

a general purpose microprocessing means for managing data flow into and out of said channel pooling signal processing means;

wherein the interconnect means connects said plurality of computing means, said testing means, and said general purpose microprocessing means; and

a digital signal processing means connected to said channel pooling signal processing means;

wherein said channel pooling signal processing means performs more computationally intensive signal processing operations and said digital signal processing means performs less computationally intensive signal processing operations.

Claim 24 (New): A base station transceiver comprising:

an antenna means for receiving communication signals; and

a signal processing means having:

a channel pooling signal processing means, including:

a reconfigurable multiprocessing means having a plurality of computing means and an interconnect means, each computing means having a data sequencing means for controlling program execution, a configurable logic means, and a dedicated memory;

a testing means for testing the function of said plurality of computing means; and

a general purpose microprocessing means for managing data flow into and out of said channel pooling signal processing means;

wherein the interconnect means connects said plurality of computing means, said testing means, and said general purpose microprocessing means; and

a digital signal processing means connected to said channel pooling signal processing means;

wherein said channel pooling signal processing means performs more computationally intensive signal processing operations and said digital signal processing means performs less computationally intensive signal processing operations.

Claim 25 (New): The signal processing apparatus of Claim 1, wherein the test interface tests the computation units for functionality and reliability while maintaining status and operating modes of all channels that are not being tested in an unchanged state.

Claim 26 (New): The method of Claim 6, wherein the test interface tests the computation units for functionality and reliability while maintaining status and operating modes of all channels that are not being tested in an unchanged state.

Claim 27 (New): The base station transceiver of Claim 9, wherein the test interface tests the computation units for functionality and reliability while maintaining status and operating modes of all channels that are not being tested in an unchanged state.

Claim 28 (New): The method of Claim 10, wherein the test interface tests the computation units for functionality and reliability while maintaining status and operating modes of all channels not being tested in an unchanged state.

Claim 29 (New): The signal processing apparatus of Claim 1, wherein each of the computation units comprise a data sequencer that controls execution of a program defining operating instructions that run in the computation unit, a customized high-speed cache for storing data received from the data sequencer, a configurable arithmetic logic unit for performing mathematical operations on data received from the cache.

Claim 30 (New): The method of Claim 6, wherein each of the computation units comprise a data sequencer that controls execution of a program defining operating instructions that run in the computation unit, a customized high-speed cache for storing data received from the data sequencer, and a configurable arithmetic logic unit for performing mathematical operations on data received from the cache.

Claim 31 (New): The base station transceiver of Claim 9, wherein each of the computation units comprise a data sequencer that controls execution of a program defining operating instructions that run in the computation unit, a customized high-speed cache for storing data received from the data sequencer, and a configurable arithmetic logic unit for performing mathematical operations on data received from the cache.

Claim 32 (New): The method of Claim 10, wherein each of the computation units comprise a data sequencer that controls execution of a program defining operating instructions that run in the computation unit, a customized high-speed cache for storing data received from the data sequencer, and a configurable arithmetic logic unit for performing mathematical operations on data received from the cache.

Claim 33 (New): The signal processing apparatus of Claim 1, wherein the computation units are configured to implement an architecture selected from the group consisting of reconfigurable logic with programmable function units, reconfigurable datapaths, reconfigurable arithmetic, and reconfigurable control.

Claim 34 (New): The method of Claim 6, wherein the computation units are configured to implement an architecture selected from the group consisting of reconfigurable logic with programmable function units, reconfigurable datapaths, reconfigurable arithmetic, and reconfigurable control.

Claim 35 (New): The base station transceiver of Claim 9, wherein the computation units are configured to implement an architecture selected from the group consisting of reconfigurable logic with programmable function units, reconfigurable datapaths, reconfigurable arithmetic, and reconfigurable control.

Claim 36 (New): The method of Claim 10, wherein the computation units are configured to implement an architecture selected from the group consisting of reconfigurable logic with programmable function units, reconfigurable datapaths, reconfigurable arithmetic, and reconfigurable control.